

**Answer all questions**

Full Marks:80  
Time : 3hours

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Section I

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1. Draw the design verification flow. Explain the meaning of the term equivalence checking and property checking with the help of reconvergence model diagrams.
2. Justify the following statement: Cycle based simulators are suitable for functional verification, while Event based simulators are suitable for timing verification.
3. Two signal lines  $r_1$  and  $r_2$  are mutually exclusive (i.e both of them cannot be high at the same time). The LTL specification of the property is :  $G[r_1 \text{ xor } r_2]$ . State true or false with justification.
4. What is the advantage of aspect orientation of 'e', as opposed to object orientation with respect to functional verification?
5. One of the practical problems in simulation based verification is the large input space. State briefly how the problem is tackled in real life.

(5x3=15 marks)

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Section II

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6. In context to language e, state briefly what is the difference between the following:
  - a) Unit and Struct
  - b) Wait and Sync

(5 marks)
7. In the following architecture (Fig 1a), the 1-hot multiplexer has a 4 bit select line encoded in 1-hot. For example, if the value in the select line is

'0010', the second input bit is selected. If by design error, the select line is not encoded in 1-hot, then the input line selected corresponds to the maximum bit position which is 1. Thus if the select line is erroneously '0011', the input bit selected is also the second. The 1-hot coded select line is generated by an internal module in the design, whose state transition diagram is shown also in the figure (Fig 1b).

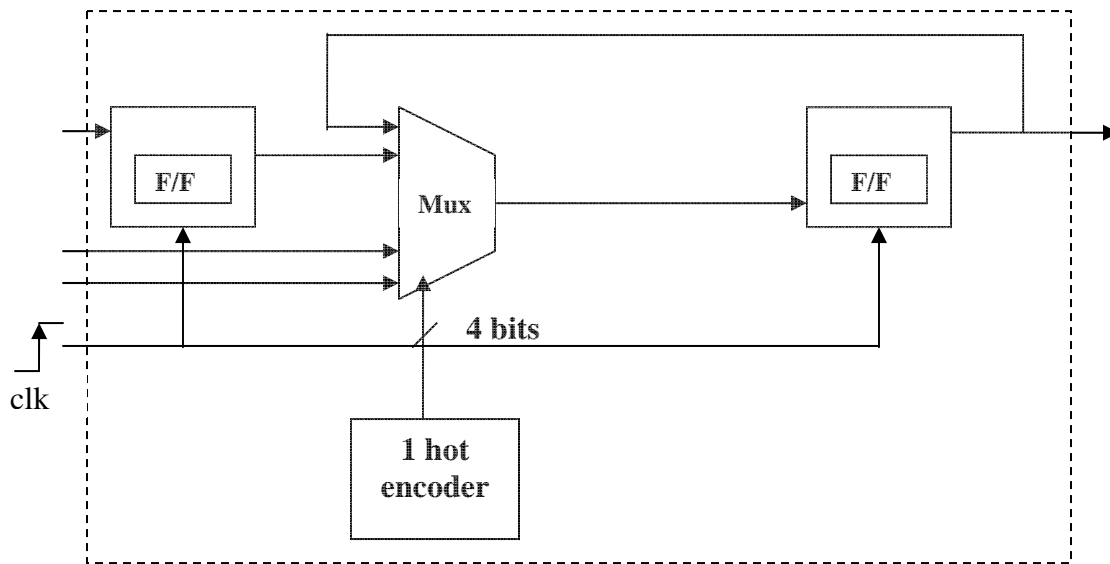


Fig 1(a): The Design (The design inside the dotted lines is not accessible from the external world)

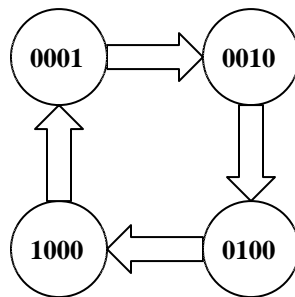


Fig 1(b): The State Transition Diagram of the 1-hot encoder

i) Device a simulation strategy (verification plan) to verify error at the output of the 1-hot encoder. Assume that the initial state of the encoder is '0010'. Compute the error detection latency (that is the number of clock cycles required between the application of the inputs and the detection of error in the output). Does the error detection latency (EDL) depend upon the initial state of the encoder? What is the maximum EDL of your verification plan? (5 marks)

ii) In order to reduce the EDL, we discussed about writing assertions in the class. Write an appropriate assertion (in any programming language) to verify that the output of the 1-hot encoder is indeed 1-hot. (5 marks)

8. A communication device receives an incoming clock up to  $M$  Hz. Write a **verilog** task to enforce this maximum frequency requirement. It should issue an error if the input frequency exceeds  $M$  Hz. (5 marks)

9. Recent trend in Computer Architecture is **multiprocessor system**. Following is the description of a two processor architecture. There are 2 processors in the system A and B. Each has its own level 1 cache. There is also a main memory to which the caches have an interface through the system bus. A requirement for such a system is that the data in both the caches must be coherent. In order to achieve this each entry in the cache has either of the three states: **exclusive, shared or modified**. A data block is in the exclusive state if the other cache does not have it. It is in the shared state if the other cache also has it. It is in the modified state if the data were modified, and thus is considered different from the copy in main memory.

Write an e-based verification environment for the following:

a) Declare e-based constructs to describe 2 caches for processors A and B and a shared memory. (Declare them as KEYED LISTS). Apart from 'data' and 'addr' fields of the keyed lists, the cache has also an extra field, 'status' which can be either: exclusive, shared or modified.

b) Write 'read' and 'write' methods to read and write the keyed lists based on the address field.

c) Add an e-snippet for the following scenario:

A initiates a read operation and there is a miss in its cache. Subsequently the cache in B is searched. If still a miss occurs, A reads from the memory, writes to its own cache and marks the data 'status' as exclusive.

(5+5+10=20 marks)

10. Using **circular queue** write a **verilog** test-bench for the following assertion:

If Req is 1, then Ack should turn 1 three clock cycles later. This causes the Req line to return to 0 seven clock cycles later. (5 marks)

11. Explain briefly (not more than 3 sentences) what do you mean by 100% functional coverage. Tabulate the minimum input table of the following expression:

$$y=(a^b)?c:1$$

If the testbench generates:  $a=0, b=1, c=0$  and  $a=1, b=0, c=1$ , what is the expression coverage achieved? (5 marks)

12. Consider the following state transition diagram (Fig 2) of the lift-controller of Building Science Block, IIT Madras which has three floors. The states are encoded using a 2 bit bus, whereas the inputs are denoted by 2 bits. There are 3 states, one corresponding to each floor, denoted by L0, L1 and L2. The state 0, denoted by L0 is the initial state. The labels on the arrows represent the valid inputs received by the controller, which can be 0, 1 or 2. Using the **state space approach** derive test scenarios to detect bugs in the state transition diagram. Based on it redraw a more correct state transition diagram which takes care of the corner cases.

(5 marks)

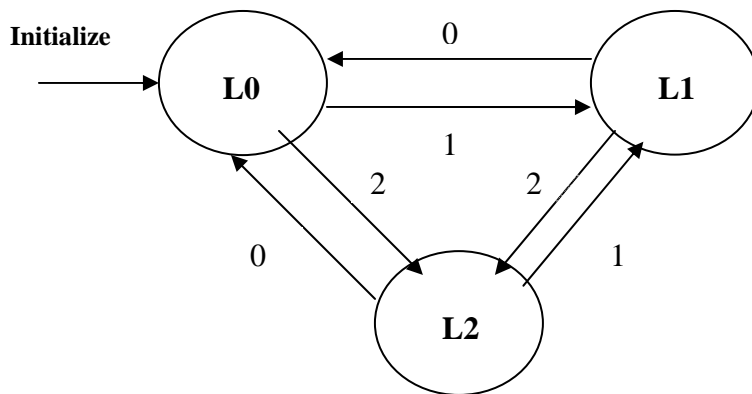


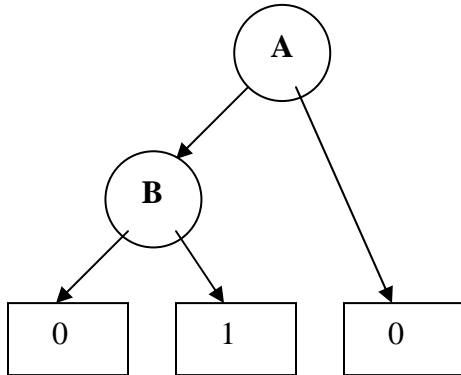
Fig 2: The State Transition Diagram of the lift controller.

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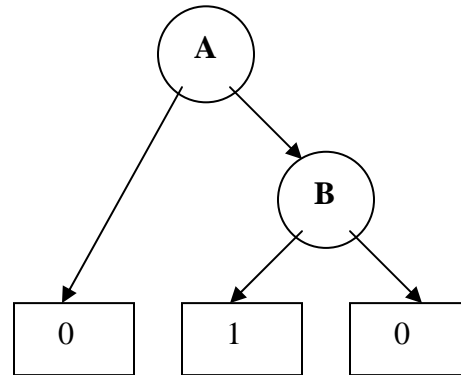
### Section III

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13. Observe the following BDDs. Use the **ITE operator** to compute the 'or' of the two BDDs X and Y. Use the variable ordering  $A < B$ . Which Boolean function does the resultant BDD represent. Use the 'swap' algorithm to interchange the ordering to  $B < A$ . Does the BDD change due to the swap? What are such type of Boolean functions called? (5 marks)



**Fig 3(a): BDD X**



**Fig 3(b): BDD Y**

14. The **resolvent algorithm** is a mathematically elegant method to check whether a Boolean function is satisfiable by splitting the problem into checking the satisfiability of resolvents, each of which has one less variable than their parent function. Using the resolvent technique check whether the following expression is satisfiable. **However do not draw a conclusion about the satisfiability until the resolvents are either constants (0 or 1) or have only 1 variable.**

$$f=(a+b+(\sim c)+d)((\sim a)+(\sim b)+c+(\sim d))(a+(\sim b)+(\sim c)+(\sim d))$$

where  $\sim a$  represents the negation of  $a$ .

Although we have an algorithm why is the Satisfiability problem considered to be a hard computer science problem? (5 marks)

15. How do you like Verification as a future research topic? Please give a frank opinion, as marks will be awarded irrespective of whether you are affirmative or negative. (1 mark)