ESI Cache Coherency Protocol Model Specification Document

1 Design

The ESI is a standard multiprocessor cache coherency protocol used in the context of several processors, each having their own cache and sharing a common global memory through a shared bus as shown in Fig. 1.

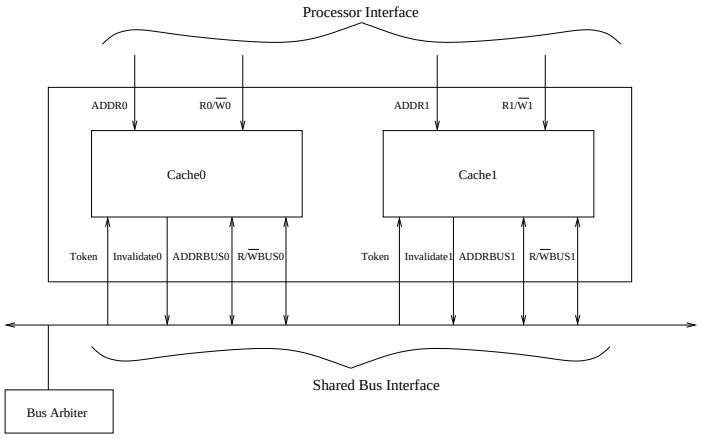

Figure 1: Processor initiated state change

The cache model for the ESI protocol consists of two caches, each having two in- terfaces, namely, the *processor interface* and the *shared-bus in- terface*, as shown in Fig. 1. The processor interface for each of the caches has two inputs to the model, namely, the ADDR (address lines corresponding to the address to be accessed by the procssor) and the R/W (Read/Write) line specifying whether the processor wants to Read or Write to the memory location specified by the ADDR lines. The caches share the bus based on a token ring protocol. Since there are only two caches in the current model, the Token is modeled as a 1-bit Toggle ip-op. When the *Token* takes the value 0, the Cache0 has control over the bus, while the Cache1 snoops the bus. Similarly, when the *Token* takes the value 1, the Cache1 has control over the bus, while the Cache0 snoops the bus.

2 Specification

This section provides specification for the cache model implemented using Verilog.

2.1 Cache Specification

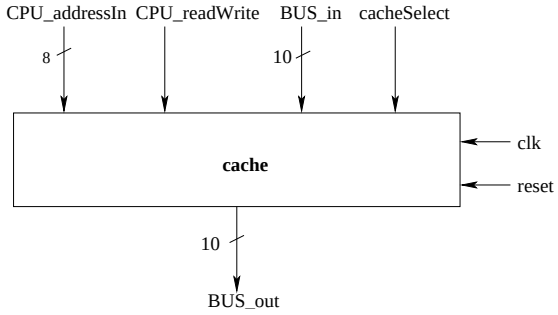

Figure 2: Cache module

SNo	Signal	Type	Size	Explanation
1	CPU_addressIn	input	8 bit	CPU Address
2	CPU_readWrite	input	1 bit	• CPU_readWrite = 1 refers to Read signal • CPU_readWrite = 0 refers to Write signal
3	BUS_in	input	10 bit	Data Bus
4	cacheSelect	input	1 bit	Token-ring signal selecting the cache
5	clk	input	1 bit	Clock signal
6	reset	input	1 bit	Reset signal for the state machines
7	BUS_out	output	10 bits	Data Bus

Table 1: Cache Signals

2.2 Top Module Specification

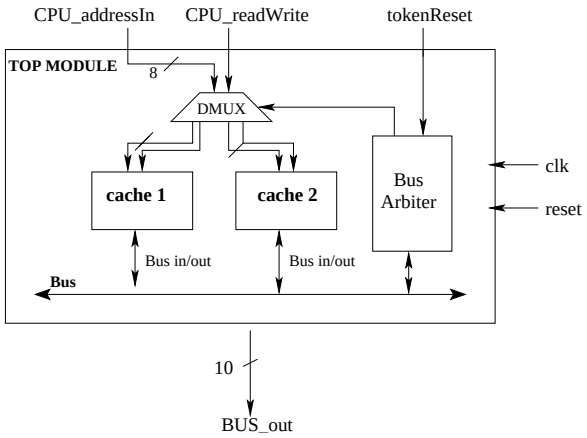

Figure 3: ESItopmodule

SNo	Signal	Type	Size	Explanation
1	CPU_addressIn	input	8 bit	CPU Address
2	CPU_readWrite	input	1 bit	• CPU_readWrite = 1 refers to Read signal • CPU_readWrite = 0 refers to Write signal
4	token_reset	input	1 bit	Reset signal for Token-ring
5	clk	input	1 bit	Clock signal
6	reset	input	1 bit	Reset signal for the state machines
7	BUS_out	output	10 bits	Data Bus

Table 2: ESItopmodule specifications

The shared-bus interface for each of the caches has the following signals.

- BUS_out are address lines used by the cache to output the address generated by the processor owning it to the shared bus, while it controls the bus
- BUS_in are address lines used to snoop the address generated by the other processor (non-owner) while not in control of the shared bus.
- Bus Arbiter implements the token-ring protocol

In the current verilog model, the address lines are 8-bit wide. The the cache state is represented in 2 bits. Hence the BUS lines are 10 bits wide. To make the model simple, in case a memory access initiated by a processor P leads to a conict (Invalidate signal raised by the cache of the other processor), it is assumed that the conict is resolved and the access initiated by P is completed within the same cycle.

3 Coherency Protocol

Every cache line/block in each of these caches can be in any one of the three states, namely, exclusive (E), shared (S), or invalid (I). The state of a cache line can be modied either due to a memory access by the processor owning it (processor-initiated) or due to some other processor (non-owner) accessing the same address stored in the cache line (bus-initiated, as it is inferred by snooping on the shared bus). The change of the state of a cache line, both processor- and bus-initiated, are modeled as state machines and shown in Figs. 1 and 2, respectively.

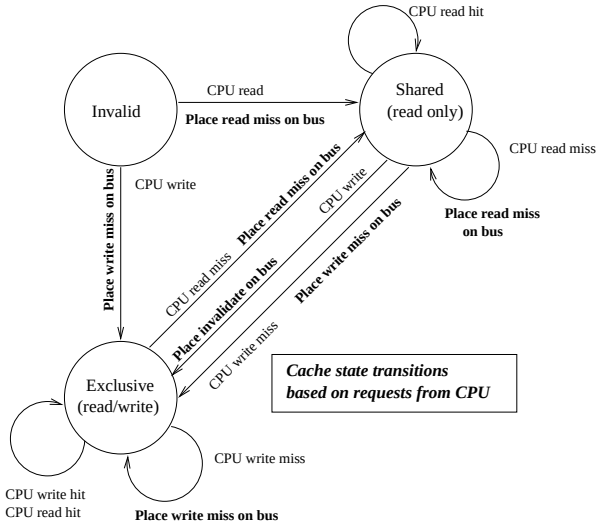

Figure 4: Processor initiated state change

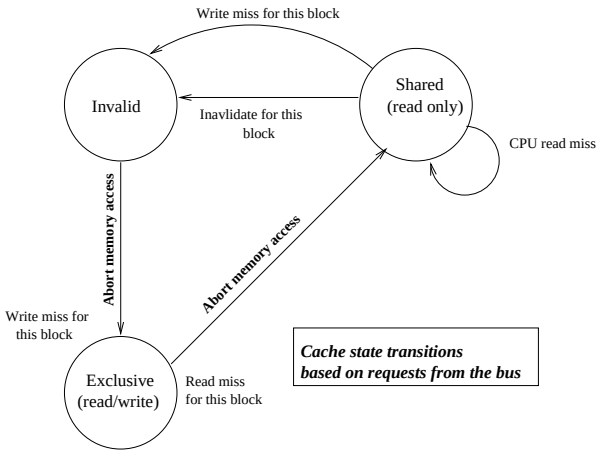

Figure 5: Bus initiated state change