RISC-V International Conference

April 2-3 2017, IIT-Madras

Sunday, 2nd April 2017

8:00 AM	**Registration**		
Session 1			
Chair : V. Kamakoti			
Time	**Event**	**Speakers**	**Affiliation**
9:00 AM	Inaugural function	V. Kamakoti	IIT- Madras
9:15 AM	Keynote-1	Dr. G.H. Rao	HCL
10:00 AM	Tea		
Session 2			
Chair : Rick O'Connor			
10:15 AM	Keynote-2: RISC-V core as a soft processor in FPGAs	Chowdhary Musunuri	Microsemi
11:00 AM	Keynote-3: Verification and Debugging for High-Assurance RISC-V	Rishiyur Nikhil	Bluespec
11:45 AM	RISC-V Business: A Configurable,Extensible RISC-V core	John Skubic	Purdue University
12:15 PM	IClass: Multi-out-of-order core based on RISC-V	Rahul Bodduna	IIT-Madras
12:45 PM	Lunch		
Session 3			
Chair : Smruti Sarangi			
1:45 PM	Keynote-4: RISC-V Going Mainstream	Rick O'Connor	RISC-V Foundation
2:30 PM	STING - A software driven portable stimulus generator for SoC design verification	Shubodeep Roy Choudury	Valtrix Technologies Private limited
3:00 PM	UVM based Verification of RISC-V based Microprocessor Architecture Using System Verilog	Gopakumar.G	Centre for Development of Advanced Computing (C-DAC)
3:30 PM	Tea		
Session 4			
Chair: Rishiyur Nikhil			
3:45 PM	Keynote-5: The Tejas Architectural Simulator	Smruti Sarangi	IIT-Delhi
4:30 PM	Early Design Space exploration of RISC-V platform for performance and Power Consumption	Deepak Shankar	Mirabilis Design
5:00 PM	U-Boot Port for RISC-V	Padmarao Begari	Microsemi India Private Ltd.

Venue: Auditorium, ICSR (Industrial Consultancy and Sponsored Research) buiding, IIT-Madras

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Session 1

Chair : G.S.Madhusudan

Time	Event	Speakers	Affiliation
9:30 AM	Keynote-6: Microsemi's Roadmap with RISC-V	Prem Arora	Microsemi
10:15 AM	Keynote-7: Addressing Performance issues of SRAM and DRAM caches. (Video Conference)	Mainak Chowdhary	IIT-Kanpur
11:00 AM	Tea		

Session 2

Chair : Prem Arora

11:15 AM	A RISC-V ISA Compatible Processor IP for SoC	Pradeep Gupta	IISc Bangalore
11:45 AM	Purdue MicroBrewer: A Microcontroller Generator	Jacob R Stevens	Purdue University
12:15 PM	RISC-V Physical Design Implementation for High Performance Applications: Challenges and Solutions	Gopakumar.G	Centre for Developement of Advanced Computing (C-DAC)
12:45 PM	Lunch		

Session 3

Chair : Chowdhary Musunuri

1:45 PM	Design of SHAKTI processor based Safety Systems for Nuclear Power Plant	M. Manimaran	IGCAR
2:15 PM	Secure Mission Critical System Design for Open Systems	Pradyumna Padhan	Hewlett Packard India Software Operations
2:45 PM	Developing Fault-Tolerant Systems with Lockstep RISC-V Softcore Processors on Non-Volatile FPGAs	Sathish Odiga	Microsemi
3:15 PM	Keynote-8: The LowRISC Platform (Video Conference)	Alex Bradbury	University of Cambridge
4:00 PM	Closing Ceremony		
4:30 PM	Tea		

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