IIT Madras Computer Architecture Initiative

RIC - 2017

RISC-V International Conference

http://rise.cse.iitm.ac.in/ric2017/index.html

ICSR Building, IIT-Madras, India

April 2nd - 3rd, 2017

CALL FOR PAPERS

Technical Program Committee

Chair:
Rick O'Connor
(RISC-V Foundation)

Members:
Krste Asanović
(UC, Berkeley)

V. Kamakoti
(IIT Madras)

G. S. Madhusudan
(IIT Madras)

Preeti Ranjan Panda
(IIT Delhi)

Mainak Chaudhuri
(IIT Kanpur)

The conference aims to advance the use of RISC-V ISA based systems across all application domains and to provide a forum for various stakeholders to share their experiences. The conference will broadly focus on the RISC-V SoC sub-systems and domain specific issues. Specific topics include, but are not limited to, the following areas:

- SoC Fabrics
- IP Blocks
- Verification Environment
- Physical Design Flow
- HW and SW Security support
- Low Power Systems
- High Performance Computing
- Safety Critical Systems
- Storage Systems.

Paper Submission

Deadline : **March 1, 2017,** at 11:59pm (Indian Standard Time)
Results : **March 5, 2017**

All papers to be submitted as PDFs to **ric17cfp@gmail.com**

Submissions should be of **at least 2 pages** (PDF format, double column, US Letter size). The authors of the paper must be clearly mentioned in the submitted paper along with email address for communication.

Authors of accepted papers will have to provide a presentation at the venue. Accepted papers and presentations will be made public on the website post the conference.